Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) Apparatus for creating a substantially DC-controllable channel bit-stream based upon a channel code, representative of a modulated signal received via a channel, the apparatus comprising means for receiving data representative of a nominal modulation transfer function or impulse response function of said channel, means for generating a synthetic high frequency signal waveform using said nominal modulation transfer function or impulse response function, means for performing threshold detection in respect of said synthetic high frequency signal waveform to produce intermediate channel bits, and means for computing a running digital sum using said intermediate channel bits.

2. (Original) Apparatus according to claim 1, wherein the code representative of the modulated signal is a run length limited (RLL) code.

3. (Original) Apparatus according to claim 2, wherein the apparatus includes means for performing RLL encoding in respect of a plurality of user bits that are to be encoded.

4. (Original) Apparatus according to claim 3, wherein said RLL encoding peformed prior to computation of the running digital sum.

5. (Previously Presented) An encoder including apparatus according to claim 1.

6. (Original) An optical data storage system, comprising an encoder according to claim 5, and a receiver comprising slicer apparatus for performing threshold detection in respect of a high frequency signal waveform derived from a modulated signal to create a digital signal representative thereof.

7. (Original) A system according to claim 6, the receiver further comprising slicer-control means for updating a threshold value in respect of the slicer apparatus in response to changes in said high frequency signal waveform, so as to correct for a DC-offset in said high-frequency signal waveform.

8. (Original) A system according to claim 6, the receiver further including a sequence detector for said high frequency signal waveform.

9. (Original) A system according to claim 8, wherein said sequence detector is a Viterbi sequence detector.

10. (Original) A method for creating a substantially DC-controllable channel bit-stream based upon a channel code, representative of a modulated signal received via a channel, the method comprising

receiving data representative of a nominal modulation transfer function or impulse response function of said channel,

generating a synthetic high frequency signal waveform using said nominal modulation transfer function or impulse response function,

performing threshold detection in respect of said synthetic high frequency signal waveform to produce intermediate channel bits, and

computing a running digital sum using said intermediate channel bits.

11. (Currently Amended) A receiver with a slicer apparatus for controlling the DC-level of a received high frequency signal waveform,

wherein said slicer apparatus performs threshold decisions in respect of said received high frequency signal waveform, and performs adjustments of the slicer-level in accordance with said threshold decisions based on minimizing ~~calculating~~ a running digital sum (RDS) signal, that is calculated at the receiver using an immediate output of the slicer, wherein the RDS signal is also calculated at the encoder ~~that~~ to generate ~~in the~~ DC-control bits in said encoder~~generation in encoding~~.

12. (Previously Presented) A receiver according to claim 11, wherein said high frequency signal waveform is a DC-controllable channel bit-stream transmitted over a channel.

13. (Currently Amended) A receiver according to claim 11, wherein said signal waveform results from a channel bit-stream transmitted over [[the]] a channel, that has been encoded by means of a method of DC-control at an encoder whereby a running digital sum (RDS) is modified such that it is not based on the exact channel bits, but on intermediate channel bits that are obtained as threshold decisions from a synthetic high frequency signal waveform.

14. (Previously Presented) A receiver according to claim 13, wherein the synthetic high frequency signal waveform is generated based on one of a nominal modulation transfer function (MTF) or its impulse response function (IRF) of the channel.

15. (Previously Presented) A receiver according to claim 13, wherein said method of DC-control at an encoder comprises the steps of:

receiving data representative of a nominal modulation transfer function or impulse response function of said channel,

generating a synthetic high frequency signal waveform using said nominal modulation transfer function or impulse response function,

performing threshold detection in respect of a synthetic high frequency signal waveform to produce intermediate channel bits, and

computing a running digital sum using said intermediate channel bits.